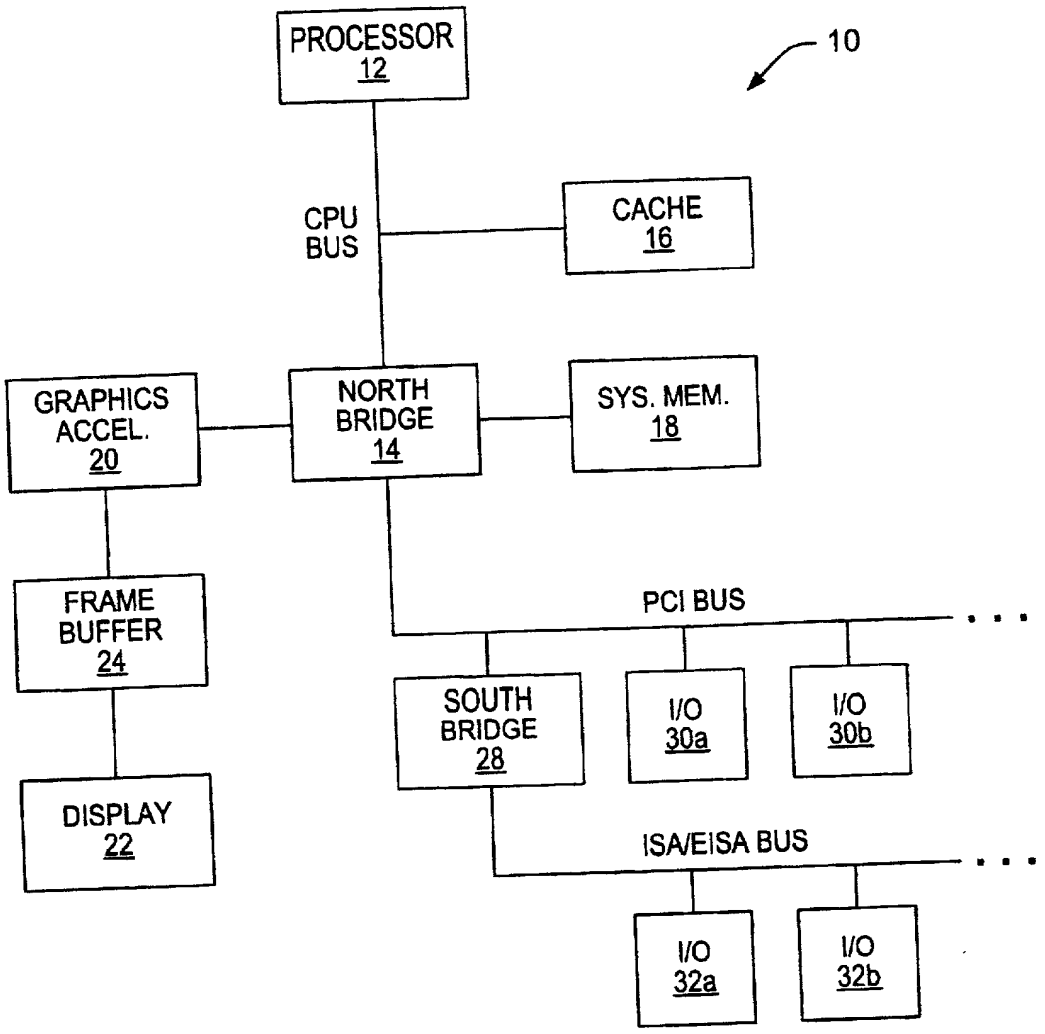

PROCESSOR
12
10
CPU
BUS
CACHE
16
GRAPHICS
ACCEL.
20
NORTH
BRIDGE
14
SYS. MEM.
18
FRAME
BUFFER
24
PCI BUS
SOUTH
BRIDGE
28
I/O
30a
I/O
30b
DISPLAY
22
ISA/EISA BUS
I/O
32a
I/O
32b

FIG. 1

System-2: Block Diagram of a Multiprocessor system incorporating Destroyer with UABM

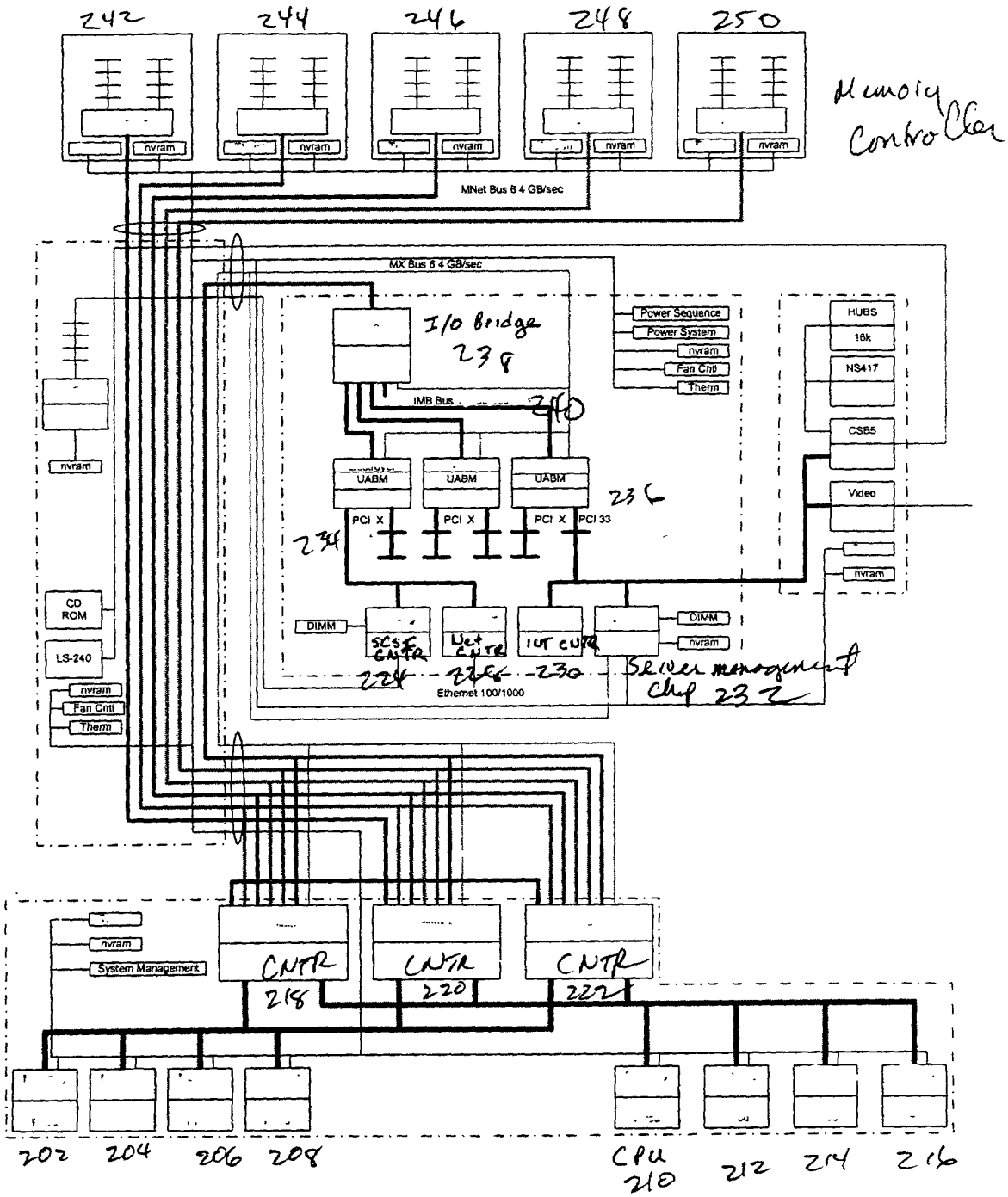


Figure 2

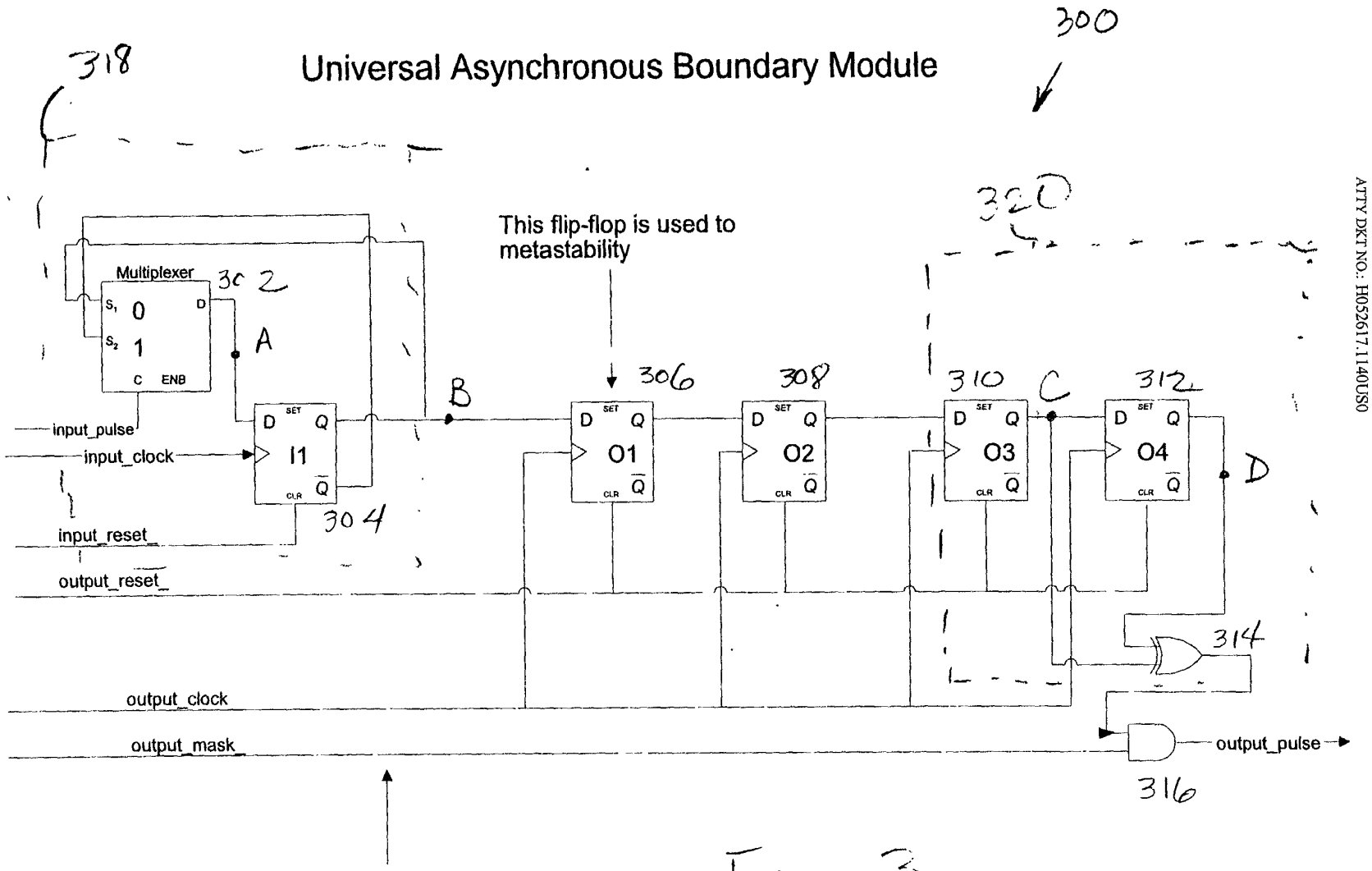
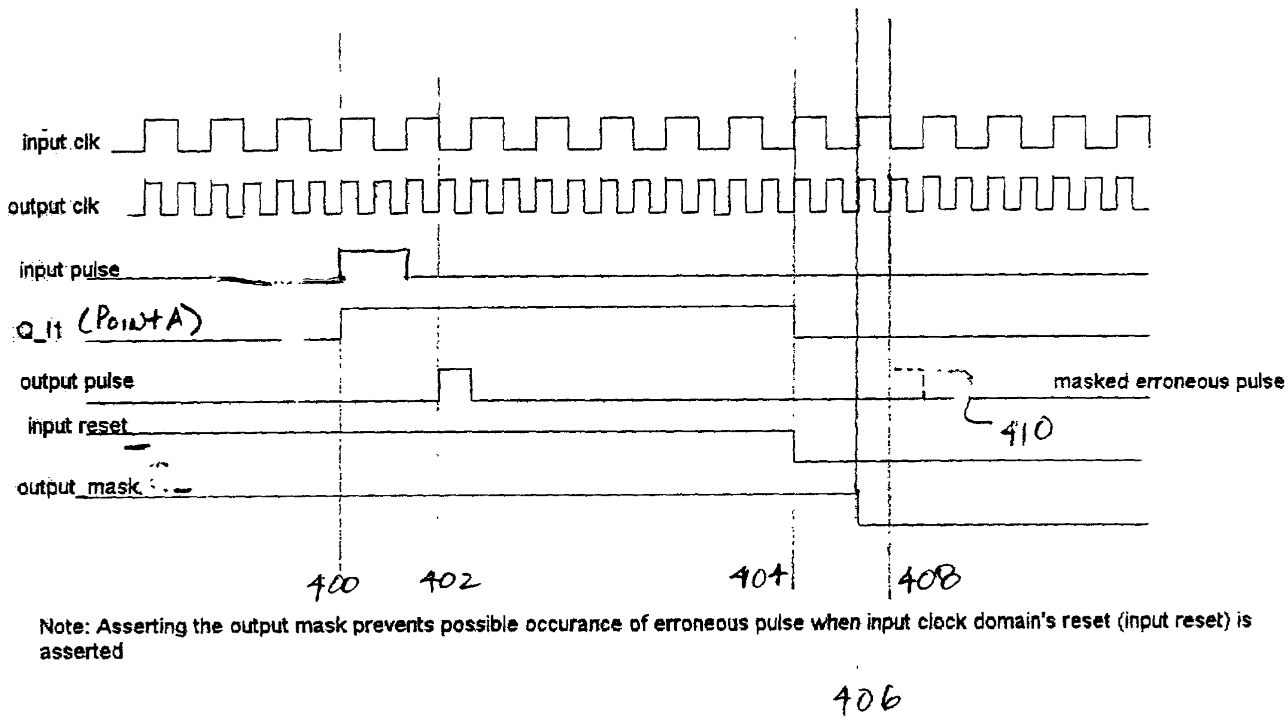


Figure 3

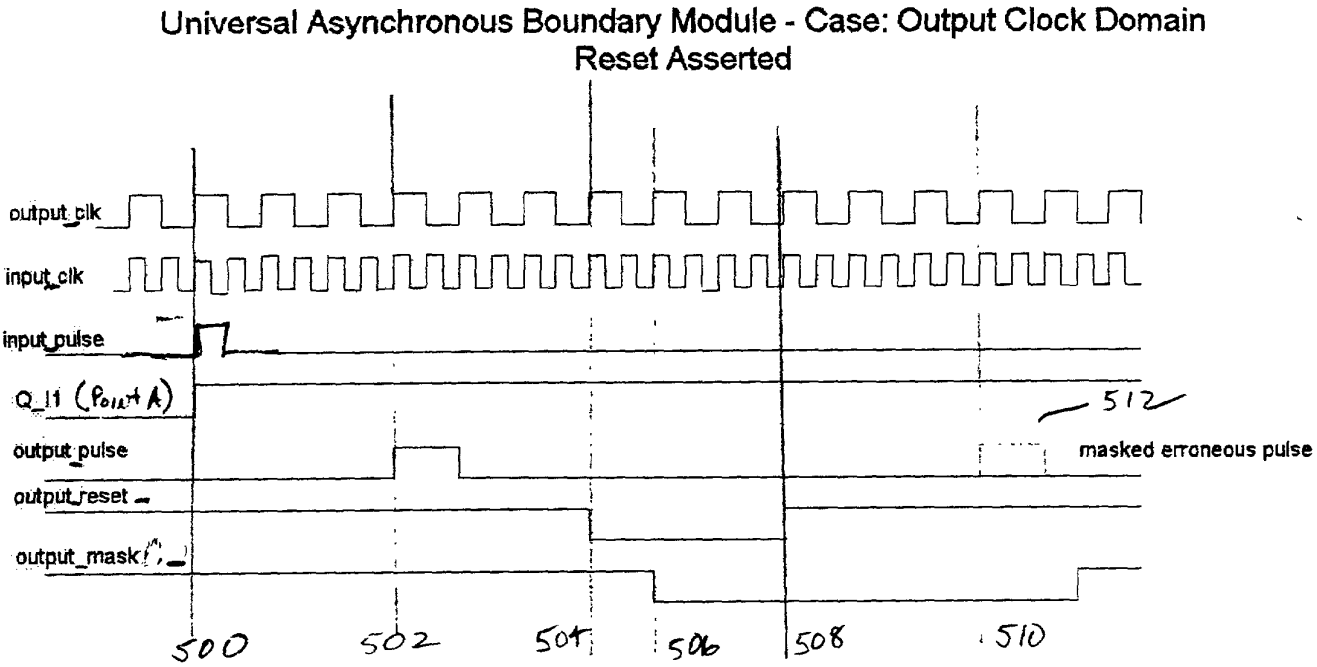
The output mask is used in where support is needed for domain to be in reset while the domain is not. It prevents output_pulses from occuring reset of hte input flip-

Universal Asynchronous Boundary Module - Case: Input Clock Domain Reset Asserted



Note: Asserting the output mask prevents possible occurance of erroneous pulse when input clock domain's reset (input reset) is asserted

Figure 4



Note: Asserting the output mask prevents possible occurance of erroneous pulse when output clock domain's reset (output reset) is asserted

Figure 5

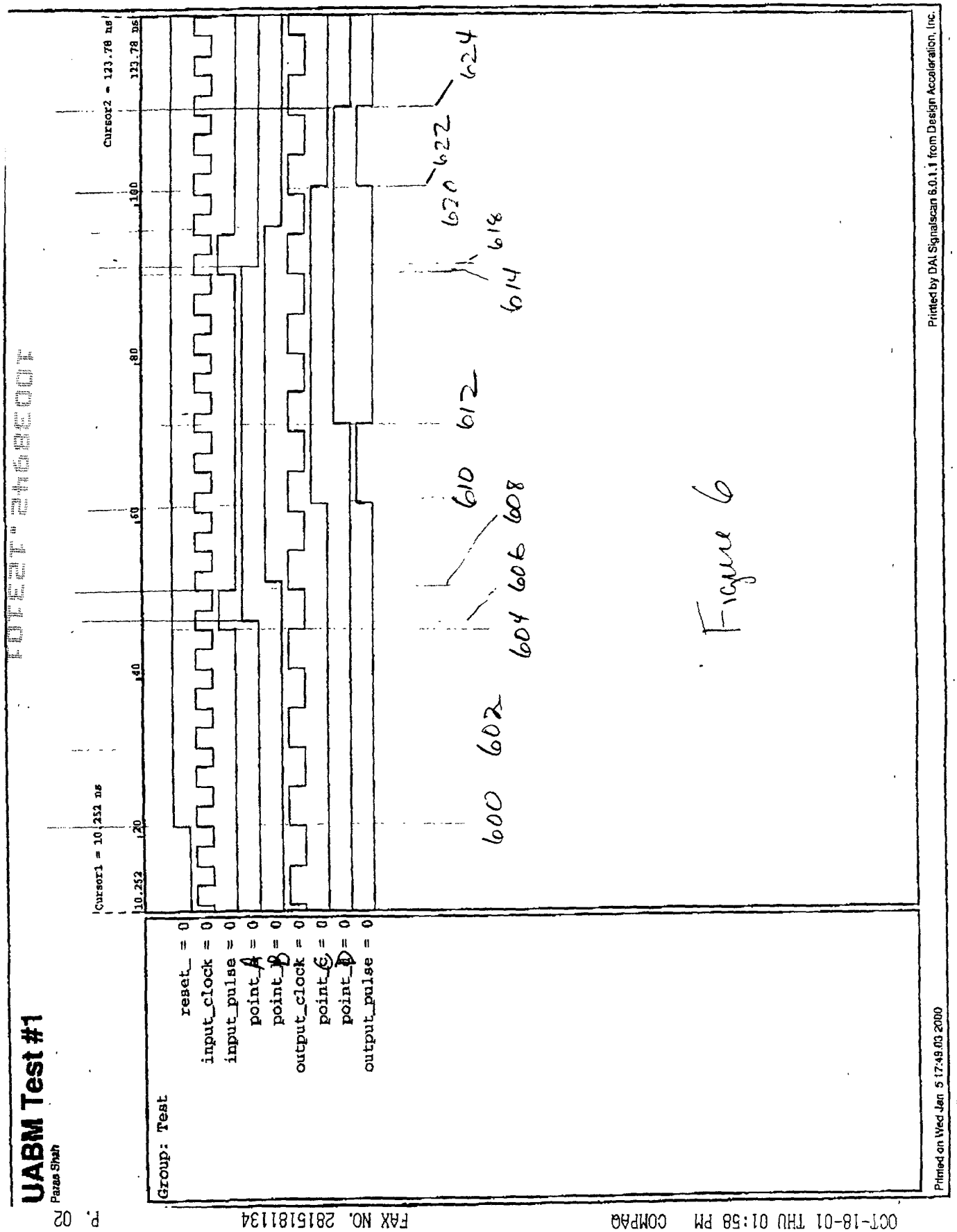

UABM Test #1
Paras Shah
Cursor1 = 10.252 ns
Cursor2 = 123.78 ns
10.252
123.78
Group: Test
reset_ = 0
input_clock = 0
input_pulse = 0
point_A = 0
point_B = 0
output_clock = 0
point_C = 0
point_D = 0
output_pulse = 0
600
602
604
606
608
610
612
614
616
620
622
624
Printed by DAI Signalscan 6.0.1.1 from Design Acceleration, Inc.
Printed on Wed Jan 5 17:48:03 2000

Figure 6

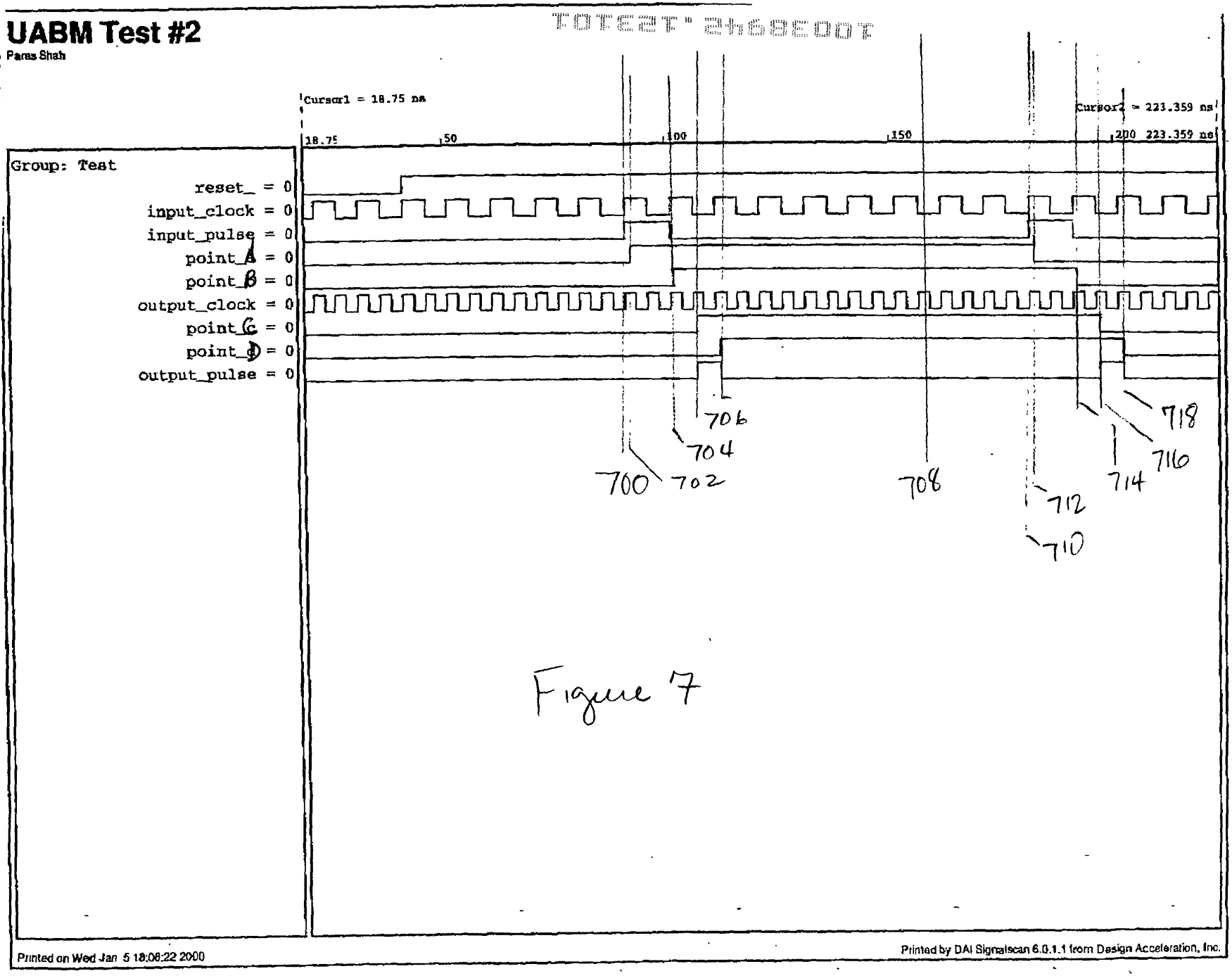
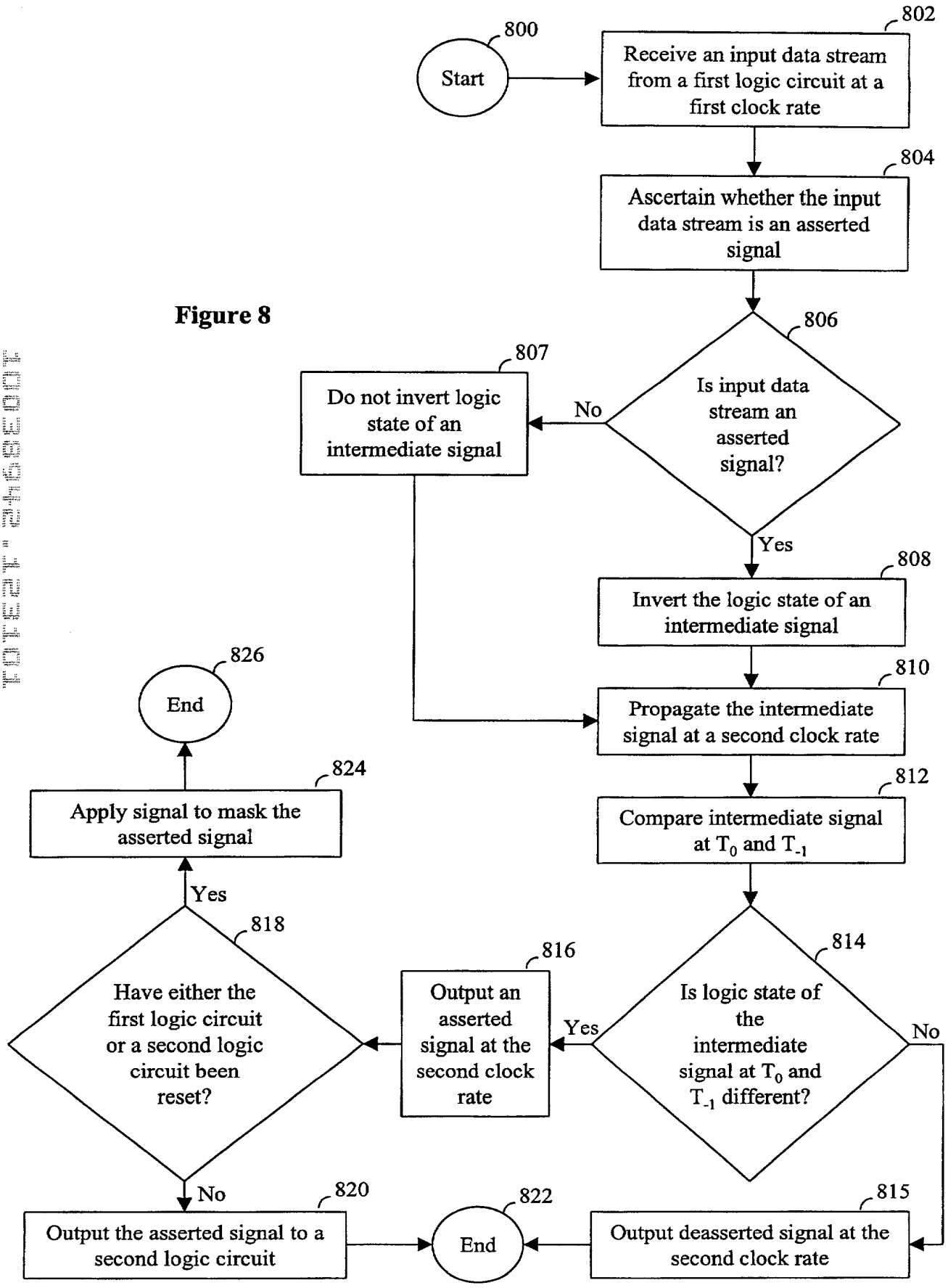

UABM Test #2
Paras Shah
Cursor1 = 18.75 ns
Cursor2 = 223.359 ns
18.75
50
100
150
200
223.359 ns
Group: Test
reset_ = 0
input_clock = 0
input_pulse = 0
point_A = 0
point_B = 0
output_clock = 0
point_C = 0
point_D = 0
output_pulse = 0
700
702
704
706
708
710
712
714
716
718
Printed on Wed Jan 5 18:08:22 2000
Printed by DAI Signalscan 6.0.1.1 from Design Acceleration, Inc.

Figure 7

Figure 8


800
Start
802
Receive an input data stream from a first logic circuit at a first clock rate
804
Ascertain whether the input data stream is an asserted signal
806
Is input data stream an asserted signal?
No
807
Do not invert logic state of an intermediate signal
Yes
808
Invert the logic state of an intermediate signal
810
Propagate the intermediate signal at a second clock rate
812
Compare intermediate signal at T_0 and T_{-1}
814
Is logic state of the intermediate signal at T_0 and T_{-1} different?
Yes
816
Output an asserted signal at the second clock rate
No
815
Output deasserted signal at the second clock rate
818
Have either the first logic circuit or a second logic circuit been reset?
Yes
824
Apply signal to mask the asserted signal
826
End
No
820
Output the asserted signal to a second logic circuit
822
End